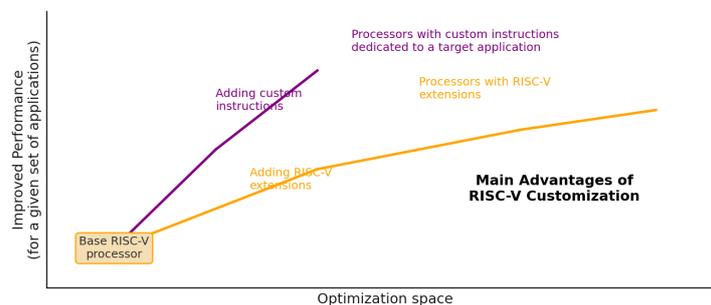


Exploring RISC-V extension capabilities for Ultra-High Field MRI systems

Research project/Bachelor/Master Thesis

Research field

Over the past decade, RISC-V has emerged as a unified solution for CPU and accelerator architectures, spanning from edge devices to the cloud, and widely adopted in academia and industry. Unlike previous architectures such as MIPS, Intel, or AMD, RISC-V defines an open standard instruction set architecture (ISA) without prescribing how the microarchitecture should be implemented (e.g., pipelining, out-of-order execution, hardware loops). This open and modular approach enables a flexible, extensible, and simple ISA that can be customized for diverse requirements while maintaining software compatibility. Among current official solutions, medical imaging, such as MRI have not yet been addressed. Although it falls within the class of high-throughput, real-time data processing applications that rely heavily on floating-point operations such as filtering and FFTs, further specialization is needed to meet the demands of Ultra-High Field Magnetic Resonance Imaging (UHF-MRI) scanners. These systems use an increasing number of channels generating pulses at up to 600 MHz, requiring ADCs capable of 3 Gs/s per channel, which produces massive data streams that must be processed and reduced in real time. To tackle these challenges, near-sensor computing offers an effective approach, and RISC-V stands out as an ideal platform for developing specialized architectures tailored to UHF-MRI needs.



Research topic and working hypothesis

In this thesis the student will start from a literature review of existing RISC-V implementation, taking into consideration the UHF-MRI requirement for its design space exploration. Then, after a pre-selection of one or more existing solutions, the student will identify architectural bottlenecks for the application and propose an architectural solution focusing on aspects such as ISA-extension, memory patterns for a targeted UHF-MRI scanner. In order to select and compare different RISC-V architectures the student has to analyze the computational requirements using analytical models like the roofline model and then propose a solution that will have impact on its plot.

Skills

Required:

- Knowledge in Verilog or VHDL
- Knowledge in C/C++, Assembly

Desired:

- Basic knowledge of EDA tools (e.g., Vivado, Cadence)
- Knowledge of Computing architecture, Parallel computing

Contact



Dr.-Ing.
Daniele Passaretti
daniele.passaretti@ovgu.de
G03-319



Scan the QR Code for
Link to the Website